Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Third Year Bachelor of Engineering (CE/IT)

(In Effect From Academic Year 2019-20)

Subject Code: CT506B-N	**Subject Title:** Advanced Computer Architecture
Pre-requisite	Computer Organization Architecture

Teaching Scheme (Credits and Hours)

Teaching scheme				Total Credit	Evaluation Scheme					
L	T	P	Total		Theory		Mid Sem Exam	CIA	Pract.	Total
Hrs	Hrs	Hrs	Hrs		Hrs	Marks	Marks	Marks	Marks	Marks
03	00	02	05	04	03	70	30	20	30	150

Course Objective:

- After successful completion of the course, student will be able to :
- understand and relate the need of parallel computer architecture
- design the memory hierarchy for parallel architecture
- evaluate the parallel architecture models
- Understand The Micro-Architectural Design Of Processors
- Learn About The Various Techniques Used To Obtain Performance Improvement And Power Savings In Current Processors

Outline of the Course:

Sr. No	Title of the Unit	Minimum Hours
1	Introduction to Computer Design and Quantitative Principles of Architecture	10
2	Instruction set principles and examples	9
3	Instruction-Level Parallelism and Its Exploitation	8
4	Multiprocessors and Thread-Level Parallelism	7
5	Memory Hierarchy Design	7
6	Storage Systems	7

Total hours (Theory): 48

Total hours (Lab): 32

Total hours: 80

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Detailed Syllabus

Sr. No	Topic	Lecture Hours	Weightage(%)
1	**Fundamental of Computer Design:** Classes of Computers, Defining Computer Architecture, Trends In Technology, Power, Energy And Cost, Dependability, Measuring, Reporting, and Summarizing Performance, Quantitative Principles of Computer Design.	10	19
2	**Instruction set principles and examples**: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set, instructions for control flow, encoding an instruction set ,the role of compiler	9	18
3	**Instruction-Level Parallelism and Its Exploitation:** ILP Concepts, Pipelining Overview ,Compiler Techniques For Exposing ILP ,Dynamic Branch Prediction ,Dynamic Scheduling , Multiple Instruction Issue ,Hardware Based Speculation ,Static Scheduling ,Multi-Threading ,Limitations Of ILP , Case Studies.	8	15
4	**Multiprocessors and Thread-Level Parallelism:** Symmetric shared memory architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared Memory and Directory-Based Coherence, Synchronization: The Basics, Models of Memory Consistency: An Introduction, Case Studies: Intel I7 Processor, SMT & CMP Processors	7	16
5	**Memory Hierarchy Design:** Cache performance, reducing cache misses penalty and miss rate, virtual memory- protection and examples of VM.	7	16
6	**Storage Systems:** Advanced Topics in Disk Storage, Definition and Examples of Real Faults and Failures, I/O Performance, Reliability Measures, and Benchmarks, A Little Queuing Theory, Designing and Evaluating an I/O System—The Internet Archive Cluster	7	16
	Total	48	100

Instructional Method and Pedagogy:

- At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
- Lectures will be conducted with the aid of multi-media projector, black board, OHP etc.
- Attendance is compulsory in lecture and laboratory which carries 10 marks in overall evaluation.
- One internal exam will be conducted as a part of internal theory evaluation.

- Assignments based on the course content will be given to the students for each unit and will be evaluated at regular interval evaluation.
- Surprise tests/Quizzes/Seminar/tutorial will be conducted having a share of five marks in the overall internal evaluation.
- The course includes a laboratory, where students have an opportunity to build an appreciation for the concepts being taught in lectures.
- Experiments shall be performed in the laboratory related to course contents.

Learning Outcome:

At The End Of The Course, The Student Should Be Able To:

- Evaluate Performance Of Different Architectures With Respect To Various Parameters
- Analyze Performance Of Different ILP Techniques
- Identify Cache And Memory Related Issues In Multi-Processors

Reference Books:

1. J.L. Hennessy, and D.A. Patterson, *Computer Architecture: A quantitative approach*, Fifth Edition, Morgan Kaufman Publication, 2012
2. J.P. Shen and M.H. Lipasti, *Modern Processor Design*,MC Graw Hill, Crowfordsville, 2005
3. Current Literature (Papers from ISCA, Micro, HPCA, ICCD, and IEEE Trans. on Computers, IEEE Architecture Letters)
4. K. Hwang and F. A. Briggs, Computer Architecture and Parallel Processing, McGraw Hill.

List of experiments

No	List of Experiments
1	Cache Simulation with Simics
2	Caches and the Memory System
3	Multiprocessors and Cache Consistency
4	Cache Coherence and Memory Ordering
5	Scalability of the Gauss-Seidel Algorithm
6	Multiprocessor Scalability
7	SIMD Instructions
8	CPU Architecture & SIMD
9	Project
10	Case Study